UNITED STATES PATENT AND TRADEMARK OFFICE

H·D

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,113	08/28/2003	Aveek Sarkar	004-8907	7868

66083 7590 10/09/2007

SUN MICROSYSTEMS, INC. c/o DORSEY & WHITNEY, LLP
370 SEVENTEENTH ST.
SUITE 4700
DENVER, CO 80202

EXAMINER	
SANDOVAL, PATRICK	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
10/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/651,113	SARKAR ET AL.	
	Examiner	Art Unit	
	Patrick Sandoval	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28 and 30-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,18-28,30-34 and 36-42* is/are rejected.

7)☒ Claim(s) *17 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to Applicant's amendment filed on 7/23/2007. Claims 1-28 and 30-42 are pending, wherein claims 1, 12, 22, 30 and 37 have been amended.

Response to Amendment

2. Applicant's amendment and remarks have been thoroughly reviewed and rejections reconsidered accordingly. However, the amendment is not considered persuasive and the applicable objections and rejections are incorporated herein.

Claim Objections

3. Claims 1, 12, 22, 30 and 37 are objected to because of the following informalities:

4. Rephrase the amended limitation "of the same circuit block design" to --of *said* circuit block design-- for proper antecedent basis.

5. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1-16, 18-28, 30-34 and 36-42 are rejected** under 35 U.S.C. 102(e) as being anticipated by Kovacs-Birkas et al. (Kovacs-Birkas) (US 7,149, 991).

8. **Pursuant to claims 1, 22 and 37**, Kovacs-Birkas discloses a method for predicting the timing response of a circuit path (Col. 1, ll. 49-67 - Col. 2, ll. 1-2, EDA tools and parasitic back annotation, Col. 3, ll. 38-43, timing analysis engine of circuit paths), a computer readable medium product and a system for performing the method, the method comprising:

obtaining a first estimated timing response of a first circuit path of a circuit block design using a first timing model (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3);

obtaining a second estimated timing response of the first circuit path of said circuit block design using a second timing model (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3);

generating a correction factor based on a variation between the first estimated timing response and the second estimated timing response (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3); and

applying the correction factor to the first timing model (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3).

9. **Pursuant to claims 2, 23 and 38**, Kovacs-Birkas discloses comprising obtaining estimated timing responses of a plurality of circuit paths using the first timing model (Kovacs-Birkas, Col. 2, ll. 28-67, Col. 3, ll. 1-17, Fig. 1, Fig. 3).

10. **Pursuant to claim 3, 24, 25 and 39**, Kovacs-Birkas discloses selecting the first circuit path from the plurality of circuit paths, wherein applying the correction factor to

the first timing model includes adjusting the estimated timing responses of the plurality of circuit paths based on the correction factor (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3).

11. **Pursuant to claims 4, 26 and 40**, Kovacs-Birkas discloses comprising generating a netlist describing the plurality of paths (Kovacs-Birkas, Col. 7, ll. 22-38).

12. **Pursuant to claim 5 and 27,** Kovacs-Birkas discloses wherein the step of obtaining a second estimated timing response includes providing the netlist to a modeling tool employing the second timing model (Kovacs-Birkas, Col. 7, ll. 22-38).

13. **Pursuant to claims 6, 28 and 41,** Kovacs-Birkas discloses wherein generating a correction factor includes comparing the first estimated timing response and the second estimated timing response (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3).

14. **Pursuant to claim 7 and 42,** Kovacs-Birkas discloses wherein applying the correction factor includes adjusting the first estimated timing response based on the correction factor (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3).

15. **Pursuant to claims 8 and 9,** Kovacs-Birkas discloses wherein the first estimated timing response includes an estimated signal propagation delay (Kovacs-Birkas, Col. 2, ll. 10-27, Col. 5, ll. 66-67, Col. 6, ll. 1-12).

16. **Pursuant to claims 10 and 20**, Kovacs-Birkas discloses wherein the correction factor includes a scaling factor (Kovacs-Birkas, Col. 10, ll. 24-49).

17. **Pursuant to claims 11 and 21**, Kovacs-Birkas discloses wherein the correction factor includes an offset (Kovacs-Birkas, Col. 9, ll. 6-14).

18. **Pursuant to claims 12 and 30**, Kovacs-Birkas discloses a method for predicting the timing response of a circuit path (Col. 1, ll. 49-67 - Col. 2, ll. 1-2, EDA tools and parasitic back annotation, Col. 3, ll. 38-43, timing analysis engine of circuit paths), and a computer readable medium product for performing the method, the method comprising:

obtaining coarse estimated timing responses for a plurality of circuit paths of a circuit block design using a first timing model, the first timing model having a first accuracy (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3);

obtaining refined estimated timing responses for one or more selected circuit paths of the plurality of circuit paths of said circuit block design using a second timing model having a second accuracy greater than the first accuracy (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3);

generating a correction factor based on the coarse estimated timing response of the one or more selected circuit paths and the refined timing estimates of the one or more selected circuit paths (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3) and

adjusting the coarse estimated timing responses of the plurality of circuit paths based on the correction factor (Kovacs-Birkas, Col. 7, ll. 39-67, Col. 8, ll. 1-58, Fig. 3)

19. **Pursuant to claim 13 and 31**, Kovacs-Birkas discloses wherein obtaining the coarse estimated timing responses includes estimating timing responses for the plurality of circuit paths using a modeling tool employing coarse timing assumptions (Kovacs-Birkas, Col. 2, ll. 28-67, Col. 3, ll. 1-17, Fig. 1, Fig. 3)

20. **Pursuant to claim 14 and 32,** Kovacs-Birkas discloses wherein obtaining refined estimated timing responses includes using a modeling tool employing refined timing assumptions (Kovacs-Birkas, Col. 2, ll. 28-67, Col. 3, ll. 1-17, Fig. 1, Fig. 3).

21. **Pursuant to claim 15 and 33**, Kovacs-Birkas discloses comprising generating a netlist describing the plurality of circuit paths (Kovacs-Birkas, Col. 7, ll. 22-38).

22. **Pursuant to claims 16 and 34**, Kovacs-Birkas discloses wherein generating a correction factor includes determining a statistical variation between the course estimated timing response of the one or more selected circuit paths and the refined timing estimates of the one or more selected circuit paths in the generation of a correction factor (Kovacs-Birkas, Col. 6, ll. 22-38).

23. **Pursuant to claims 18**, Kovacs-Birkas discloses wherein the coarse estimated timing responses include an estimated signal propagation delay (Kovacs-Birkas, Col. 2, ll. 10-27, Col. 5, ll. 66-67, Col. 6, ll. 1-12).

24. **Pursuant to claims 19**, Kovacs-Birkas discloses wherein the coarse estimated timing responses include an estimated signal propagation time (Kovacs-Birkas, Col. 2, ll. 10-27, Col. 5, ll. 66-67, Col. 6, ll. 1-12).

25. **Pursuant to claim 36**, Kovacs-Birkas discloses wherein the computer readable medium is selected from a group consisting of a random access memory, a read only memory, a magnetic tape, a magnetically encodable disk, an optically encodable tape, and an optically encodable disk (Kovacs-Birkas, Col. 4, ll. 64-67, Col. 5, ll. 1-2, wherein a RAM, ROM magnetic tape, etc. are inherent to a computer readable medium).

Allowable Subject Matter

26. **Claims 17 and 35** contain allowable subject matter.

27. **Claims 17 and 35** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

28. The following is a statement of reasons for the indication of allowable subject matter:

29. **Pursuant to claims 17 and 35**, in a method of designing, analyzing and comparing timing models, and a computer readable medium product for performing the method, the prior art does not fairly teach or suggest:

generating a correction factor for each of the plurality of circuit paths, wherein the statistical variation is equal to a standard deviation of the correction factors for the plurality of circuit paths divided by mean of the correction factors for the plurality of circuit paths; and

adjusting the coarse estimated timing responses of each of the plurality of circuit paths individually, if the statistical variation exceeds twenty percent.

Remarks

30. The objections to claims 12, 17 and 35 have been removed in light of Applicant's amendment filed 7/23/2007.

31. **Pursuant to independent claims 1, 12, 22, 30 and 37**, Applicant argues (See Remarks, Pages 8-9) that Kovacs-Birkas does not disclose measurement of *the same circuit path* using two different timing models, and that a circuit path measured is not the same path when more accurate, distributed parasitics are available.

32. The Examiner is not persuaded.

33. Kovacs-Birkas discloses extracting wiring parasitics of nets in order to account for complete resistive, capacitive and inductive effects on signal delay of interconnect paths (Kovacs-Birkas, Col. 1, ll. 49-67). The extracted wiring parasitics are back annotated (Kovacs-Birkas, Col. 2, ll. 1-2) into a circuit under evaluation along each path, as defined by the structure of an integrated circuit under evaluation (Kovacs-Birkas, Col. 3, ll. 38-43), for the timing analysis engine of Kovacs-Birkas to use in order to evaluate circuit performance. It is well known in the art to incorporate extracted parasitic data into a design simulation, as by doing so one may most accurately portray circuit performance for designer evaluation. Accurate modeling of circuit performance is very important, because as minimum feature sizes of integrated circuits continue to shrink, the ratio of interconnect delay to total delay has increased substantially and must be considered (Col. 1, ll. 58-66).

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

35. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick Sandoval whose telephone number is 571-272-7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov., Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Patrick Sandoval
Patent Examiner
Art Unit 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER